Electronics Design Checklist Originally By Hank Wallace

This is a checklist for electronics designers. The idea is for engineers and technicians to share experiences and create a detailed checklist which the individual designer can pare down to meet his or her specific needs. There are many details that go into the making of a first-run design success, and this checklist helps prevent Murphy's gremlins from marring an otherwise healthy design.

How do you use this checklist?

1. Make a copy of the list on your computer. Edit the rules to conform to your company's practices and delete the rules that do not apply to your work.
2. Discuss the checklist with others you work with, adding items from their experience. For maximum benefit, get their commitment to use it, too.
3. Make the checklist part of your design review and design release procedures. Do not release a product for prototyping or manufacturing until each checklist item has been verified.
4. Keep the original checklist for each release or revision so you can close the loop on the process, adding some items later if needed. For each design error that occurs, add an item to the list.
5. Contribute your suggestions for additions or changes so others can benefit from your experience. Suggestions? Send feedback to jeff@jldsystems.com and EE Expert Hank Wallace.

THANKS to all the readers who have contributed to this checklist over the years. You have helped reduce the incidence of gastrointestinal distress among engineers worldwide.

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1. Electronic and Schematics
    - all unused inputs terminated
    - race conditions checked
    - Darlington outputs (1.2v low) driving logic inputs
    - mating connectors on different assemblies checked for same pinout
    - all outside world I/O lines filtered for RFI
    - all outside world I/O lines protected against static discharge
    - bypass cap for each IC
    - voltage ratings of components checked
    - each IC has predictable or controlled power-up state
    - file name on each sheet
    - dot on each connection
    - minimum number of characters in values
    - consistent character size for readability
    - schematics printed at a readable scale
    - all components have reference designators and values

- special PCB or parts list information entered for each component, if required
- polarized components checked
- electrolytic and tantalum capacitors checked for no reverse voltage
- power and ground pins listed for each component with hidden power pins
- check hidden power and ground connections
- title block completed for each sheet
- ground made first and breaks last for hot pluggability
- pullups on all open collector outputs
- sufficient power rails for analog circuits
- LM324 and LM358 outputs loaded to prevent crossover distortion
- amplifiers checked for stability
- oscillators checked for reliable startup
- consider signal rate-of-rise and fall for noise radiation
- check for input voltages applied with power off and CMOS latchup possibilities
- reset circuit design reliable, both glitch-free and consistent; tested with slow power supply fall time
- separate analog signals from noisy or digital signals
- ability to disable watchdog timer for testing and diagnostics and emulation
- sufficient capacitance on low dropout voltage regulators
- setup, hold, access times for data and address busses
- check the data sheet fine print and apnotes for weird IC behaviors
- determine effect of losing each of multiple grounds on a connector
- automotive powered devices must withstand 60 to 100 volt surges
- check maximum power dissipation at worst-case operating temperatures
- check time delays and slew rates of opamps used as comparators
- check opamp input over-drive response for unintended output inversion
- check common mode input voltages on opamps
- check for voltage transients and high voltages on FET gates
- check failure modes and effects of failed power semiconductors
- estimate total worst case power supply current
- check pin numbers of all custom-generated parts
- for buses, ensure bus order matches device order
- ensure resistors are operating within their specified power range plus safety factor
- resistor power ratings derated for elevated ambient temperatures
- electrolytic/tantalum capacitor temperature/voltage derating sufficient for MTBF
- check for low impedance sources driving tantalum caps which can cause premature failure
- avoid reverse base-emitter current/voltage on bipolar transistors
- use of baud rate friendly clock source for devices that have serial ports
- ~IOR and ~IOW strobes on UARTs are typically incompatible with timings of signals readily available on many processors
- ROHS compliance requirement review

- part obsolescence review
- replacement part compatibility with software requirements: "top-boot vs. bottom boot FLASH", UART compatibility, SPI memory timing and addressing for different sized parts
- all PCB signal changes noted to the software geeks
- all no-connect pins on IC's should be labelled NC
- text should not overlap wire or symbol graphics on schematics
- busses with off-page destinations present with title at page margin
- card edge connectors identify mating part
- page title present and consistent on all pages if not in title block
- under-utilization of gates on multi-gate parts checked
- off board connectors identify all signals even if not used on this design
- unpopulated parts annotated and enclosed by dashed-line box on schematics
- wires exist between all connected pins/ports (no direct pin/pin connections) if capture package does not like such connections
- symbols identify open collector/drain pins and internal pulled up/down pins
- clock lines with series termination and parallel termination component locations present even if not populated; zero ohm resistor for series, unpopulated parts for parallel termination
- avoid direct connect of mode pins or no-connect bus lines to GND or VCC so PCB rework options are maximal
- diagnostic resources by design (leds, serial ports, etc.) even if unpopulated by default
- pin names and attributes on symbols with multi-function pins should match actual design usage (I/O/Bi, Name)
- connect DIP switches and other grouped I/O to ports in a logical way, LS bit to LS bit, MS bit to MS bit
- preferred component reference designators
    - R fixed resistor
    - RN resistor network
    - RV variable resistor
    - C capacitor (network, fixed or variable)
    - L inductor
    - Q transistor, FET, SCR, TRIAC
    - D,CR diode, rectifier, Zener, varicap, LED
    - DL multisegment display (any type)
    - VR,Q,IC voltage regulator
    - U,IC integrated circuit
    - J socket, jack (female)
    - P plug (male)
    - JP jumper (pins, trace, or wire)
    - Y,X crystal
    - M modular subassembly, daughter board
    - S mechanical switch
    - F fuse

        - FL filter
        - T transformer
        - KB keyboard
        - B,BT battery
2. PCB Design
    - hole diameter on drawing are finished sizes, after plating.
    - finished hole sizes are >=10 mils larger than lead
    - silkscreen legend text weight >=10 mils
    - pads >=15 mils larger than finished hole sizes
    - place thruhole components on 50 mil grid
    - no silkscreen legend text over vias (if vias not soldermasked) or holes
    - soldermask does or does not cover vias
    - all legend text reads in one or two directions
    - components labeled left-right, top-bottom
    - company logo in silkscreen legend
    - company logo in foil
    - copyright notice on PCB
    - date code on PCB
    - PCB part number
    - assembly part number on PCB
    - all polarized components point same way
    - components >=0.2" from edge of PCB
    - ground planes where possible
    - test pad or test via on every net to allow in circuit test
    - test pads 200 mils from edge of board
    - mounting holes electrically isolated or not
    - mounting holes with or without islands
    - proper mounting hole clearance for hardware
    - all polarized components checked
    - no acute inside angles in foil
    - traces >= 20 mils from edge of PCB
    - PCB revision on silkscreen legend
    - assembly revision blank on silkscreen legend
    - serial number blank on silkscreen legend
    - soldermask swell checked
    - thru hole drill tolerance noted
    - thru hole soldermask tolerance noted
    - thru hole route tolerance noted
    - thru hole silkscreen legend tolerance noted
    - drill legend shows all symbols and sizes
    - mounting holes matched 1:1 with mating parts
    - automated netlist check
    - manual netlist check
    - check netlist for nodes with only one connection
    - CAD design rule check
    - drill origin is a tooling hole

- checkplots sent with disk based photoplot files
- NC drill and photoplot file language format noted
- tools on drill plot and NC drill file cross checked
- soldermask over bare copper noted if needed
- PCB thickness, material, copper weight noted
- trace and space geometry noted
- printed drill report sent with checkplots
- printed aperture table sent with checkplots
- photoplot files checked in file viewer
- test coupon on PCB containing minimum geometry features
- trace width sufficient for current carried
- minimum component body spacing
- SMD pad shapes checked
- visual references for automated assembly
- tooling holes for automated assembly
- sufficient clearance for high voltage traces
- component and trace keepout areas observed
- high frequency circuitry precautions observed
- thermal reliefs for internal power layers
- solder paste mask openings are proper size
- blind and buried vias allowed on multilayer PCB
- PCB layout panelized correctly
- panelized PCB fits test and manufacturing equipment
- sufficient clearance for socketed ICs
- SMD component orientation arbitrary or consistent
- ensure pin 1 interpretation and orientation consistent among all connectors of a given type on the board
- clearance for IC extraction tools
- clearance for emulator adapter or pod
- clearance for sockets for ICs during proto phase
- standoffs on power resistors or other hot components
- digital and analog signal commons joined at only one point
- EMI and RFI filtering as close as possible to exit and entry points in shielded areas
- layout PCB so that any rework or repair of a component does not require removal of other components
- extra connector and IC pins accessible on prototype boards, just in case
- check all power and ground connections to ICs
- provide ground test points, accessible and sized for scope ground clip
- potentiometers should increase controlled quantity clockwise
- check hole diameters for odd components: rectangular pins, spring pins
- check the orientation of all connectors using actual connector/cable
- bypass capacitors located close to IC power pins
- all silkscreen text located to be readable when the board is populated
- all ICs have pin one clearly marked, visible even when chip is installed

- high pin count ICs and connectors have corner pins numbered for ease of location
- silk screen tick marks for every 5th or 10th pin on high pin count ICs and connectors
- verify that all series terminators are located near the source
- place I/O drivers near where their signals leave the board
- high frequency crystal cases should be flush to the PCB and grounded
- check for traces running under noisy or sensitive components
- check IC pin count on layout vs schematic
- no vias under metal-film resistors and similar poorly insulated parts
- check for traces which may be susceptible to solder bridging
- maximize distances between features where possible
- check for dead-end traces
- check for power not shorted to ground
- ensure schematic software did / did not separate Vcc from Vdd, Vss from GND as needed
- provide multiple vias for high current and/or low impedance traces
- coupons for board part number, anti-static warning, QC markings
- PCB has ground turrets, power rail test points, and test points for for important signals, all labeled

3. PCB Assemblies
   - miscellaneous parts on bill of materials and assembly notes for same: hardware, heat sinks, heat sink compound or composite insulators, IC sockets, consumables
   - assembly notes for all special operations
   - conformal coating
   - special static handling precautions required during assembly and test
4. Wired Assemblies
   - wire gauge checked for compatibility with each termination
   - cable ties or lacing cord shown where needed
   - length &color of each wire indicated
   - notes about application of wire terminations (technique, heat shrink tubing, amount of solder, crimp force, tools, etc.)
5. Parts Lists
   - each component has quantity, reference designator and description
   - list qualified part numbers for special devices
   - suggested and alternate manufacturer(s) listed
   - object/binary code and method/programmer specified for each programmable device
   - price and availability checked for each component
6. Mechanical Drawings
   - standard title block and border used
   - no dimensions on the material
   - every feature must have X and Y dimension, along with radius, diameter, etc.

    - every hole must be checked for alignment with mating hole(s) in other parts
    - check every hole diameter
    - tolerance for sheet metal feature position noted
    - tolerance for sheet metal hole size noted
    - specify material
    - specify finish
    - specify units
    - specify debur or brush
    - details for special operations
    - file name on each sheet
    - CAD layers shown on drawing
    - all hardware specified and listed on parts list
    - screw lengths checked; extra thread required for fasteners (nut, lockwasher, washer)
    - hole diameters checked for each screw
    - tapped hole thread details indicated
7. Software
    - each version archived for future reference
    - loops checked for terminating conditions
    - communications timeouts checked
    - all branches tested
    - revision history noted for all changes
    - CPU utilization measured
    - interrupt response time measured
    - interrupt execution time measured
    - naming conventions consistent and relevant to humans
    - adherence to coding style standards
    - power-up, power-down considerations
    - unused vectors trapped to restart or damage control routine
    - unused ROM space loaded with trap or restart instructions
    - warm and cold reset differences
    - nonvolatile memory corruption possibilities checked during power-up, power-down, and program-gone-wild conditions
    - design notes within or separate from code
    - check for FIFO and buffer overruns
    - check critical timer driver code
    - check for odd address usage on 16/32 bit micros, especially an odd stack pointer
    - use a LINT utility on C programs to find subtle problems
    - program's data structures contain version numbers to detect program version upgrades and translate the structures' formats
8. Testability
    - test points on PCBs for critical circuits, hard to reach nets
    - test pads for in-circuit or bed-of-nails functional testing
    - test pads on a regular grid

- test procedure written for each test phase
- special test arrangements and connectors for testing

9. Maintainability
    - easy disassembly and reassembly
    - fuses accessible and labeled
    - self test mode
    - spare parts available
    - status LEDs on PCB
    - event logging of exceptional conditions
    - vibration tolerance of entire assembly and individual modules
    - surge current magnitude through semiconductors within rating
    - thermal cycling excursions internal to components and assemblies within acceptable limits
    - capacitors mounted below or away from heat-dissipating devices such as transformers
    - resistance and tolerance of entire product to static discharge via any path
10. Safety
    - fuse and circuit breaker size and characteristics
    - fuse sizes marked near fuse holder
    - room to remove fuse without damaging other components
    - spare fuse storage
    - shock hazards
    - radiated energy warnings and shields
    - applicable standards checked
    - protection against liquids and foreign objects
11. Documentation
    - end-user instructions: unpacking, how to use, warranty, service, troubleshooting
    - service manual: troubleshooting procedures, parts lists, helpline info
    - design notes: why significant design decisions were made the way they were
    - other info that may be lost if designers depart the organization